



Form 1449 (Modified) Information Disclosure Statement By Applicant (Use Several Sheets if Necessary)	Atty Docket No.	Application No.:
	NOVLP068/NVLS-2818	10/690,084
	Applicant:	
	Koos et al.	
	Filing Date	Group
	October 20, 2003	1765

U.S. Patent and Publication Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
/LV/	A1	7,008,871	03/2006	Andricacos et al.			
	A2	5,913,147	06/1999	Dubin et al.			
	A3	6,136,707	10/2000	Cohen			
	A4	5,891,513	04/1999	Dubin et al.			
	A5	6,065,424	05/2000	Shacham-Diamond et al.			
	A6	5,969,422	10/1999	Ting et al.			
	A7	5,972,192	10/1999	Dubin et al.			
	A8	5,576,052	11/1996	Arledge et al.			
	A9	5,151,168	09/1992	Gilton et al.			
	A10	5,674,787	10/1997	Zhao et al.			
	A11	6,197,181	03/2001	Chen			
	A12	4,981,725	01/1991	Nuzzi et al.			
	A13	5,318,803	06/1994	Bickford et al.			
	A14	6,398,855	06/2002	Palmans et al.			
	A15	5,382,447	01/1995	Kaja et al.			
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	A18	2004/0065540	04/2004	Chebiam et al.			
	A19	6,645,567	11/2003	Mayer et al.			
	A20	2003/0075808	04/2003	Inoue et al.			
	A21	4,737,446	04/1988	Cohen et al.			
	A22	6,887,776	05/2005	Shang et al.			
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Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
/LV/	B1	99/47731	09/23/99	WIPO			X	
Examiner /Lan Vinh/				Date Considered 03/21/2007				

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
/LV/	C1	U.S. Office Action mailed January 23, 2007, from U.S. Application No. 11/251,353. [Atty. Dkt. No. NOVLP141/NVLS-3107]
	C2	Andryuschenko et al., "Electroless and Electrolytic Seed Repair Effects on Damascene Feature Fill," Proceedings of International Interconnect Tech. Conf., San Francisco Ca., June 4-6, 2001, pp 33-35
	C3	Chen et al., "ECD Seed Layer for Inlaid Copper Metallisation," Semiconductor Fabtech - 12 th Edition, 5 Pages, July 2000.
	C4	Ken M. Takahashi, "Electroplating Copper into Resistive Barrier Films," Journal of the Electrochemical Society, 147 (4) 1417-1417 (2000)
	C5	T.P. Moffat et al., "Superconformal Electrodeposition of Copper in 500-90 nm Features," Journal of the Electrochemical Society, 147 (12) 4524-4535 (2000)
	C6	Ritzdorf et al., "Electrochemically Deposited Copper," Conference Proceedings ULSI XV 2000, Materials Research Society, 101-107
	C7	Reid et al., "Optimization of Damascene Feature Fill for Copper Electroplating Process," Shipley Company, IITC 1999, 3 Pages
	C8	Reid et al., "Copper PVD and Electroplating," Solid State Technology, July 2000, www.solid-state.com , 86-103
	C9	Reid et al., "Factors Influencing Fill of IC Features Using Electroplated Copper," Adv Met Conf Proc 1999, MRS 10 Pages, (2000)
	C10	Shacham-Diamond et al., "Copper Electroless Deposition Technology for Ultr-Large-Scale-Integration (ULSI) Metallization," Microelectronic Engineering 33 (1997) 47-58
	C11	Hu et al., "Effects of Overlayers on Electromigration Reliability Improvement for Cu/Low K Interconnects," Presented in the Proceedings of the 42 nd Annual IRPS held April 25-29, 2004, page v, article published May 28, 2004, 7 Pages.
↓	C12	Park et al., "Electroless Layer Plating Process and Apparatus", Novellus Systems, Inc., Application No. 10/235,420, filed September 30, 2002 [Atty. Dkt. No. NOVLP049/NVLS-2677]
/LV/	C13	U.S. Office Action dated September 1, 2005 for Application No. 10/235,420 [Atty. Dkt. No. NOVLP049/NVLS-2677]
Examiner /Lan Vinh/		Date Considered 03/21/2007

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